Digital Logic Design Laboratory

Lab 3

MSI Combinational Logic (II)

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# I. Objectives

In this laboratory, students will study:

- Understand the operation of combinational logic circuit.

- The operation of some combinational ICs such as: full adder, decoder, encoder.

# II. Procedure

1. Design the adder with two one-bit binary.

a. Design the half adder two one-bit binary.

Two inputs are A, B. Two outputs are S and C.

Build the truth table and the expressions

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | S | C |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

The simplified expressions:

S = A⊕B (XOR gate)

C = A.B (AND gate)

Implement the circuit via simulation software and paste the result in here

A diagram of a circuit

Description automatically generated

Make comment on the results

The sum (S) is 1 when the number of input bits that are 1 is odd.

The carry (C) is 1 only when both input bits are 1

b. Design the full adder two one-bit binary.

Three inputs are Cin, A, B. Two outputs are S and Cout.

Build the truth table and the expressions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Cin | S | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The simplified expressions:

S = (A⊕B) ⊕ C

Cout = AB + (A⊕B) ⊕ C

Implement the circuit via simulation software and paste the result in here

A screenshot of a computer

Description automatically generated

Make comment on the results

The first two inputs are labeled A and B, while the third input is called C-IN. The output provides a SUM, and C-OUT is activated only when two or more of the three inputs are in a HIGH state. Thus, C-OUT will be activated under these circumstances.

2. 8-to-3 Priority Encoder (Interrupt sorter) – IC 74HC148

a. Investigate IC – 74HC148

Construct the circuit as below:

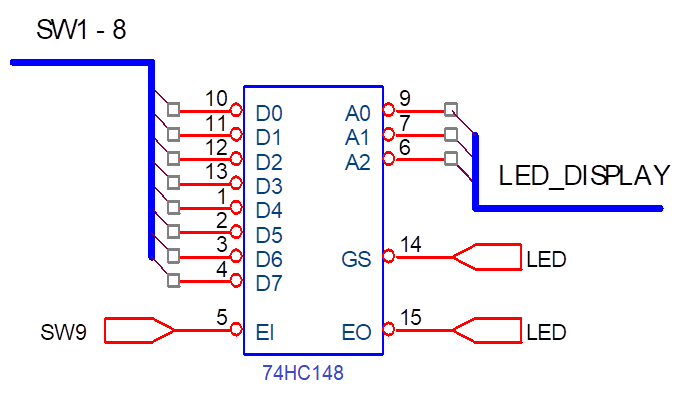


Figure 1 – Encoder 8-to-3 IC 74LS148

- The outputs are connected to LED displays to determine the logic levels.

- Choose the input data D0 - D7 by switches in the order from SW0 to SW7.

- Control EI by using switch.

- Observe the results and fulfill the truth table of 74HC148.

- What are the functions of  and ?

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | | | | | | | | | Output | | | | |
| EI | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | GS | A2 | A1 | A0 | E0 |
| 1 | X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | X | X | X | X | X | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | X | X | X | X | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | X | X | X | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a circuit board

Description automatically generated

b. Priority encoder

Let’s EI equal to 0, fill the outputs A2, A1, A0 in the following cases

|  |  |  |  |
| --- | --- | --- | --- |
|  | A2 | A1 | A0 |
| Case 1:  I3 = I2 = I1 = 0  I7 = I6 = I5 = I4 = I0 = 1. | 0 | 0 | 1 |
| Case 2:  I7 = I2 = 0.  I6 = I5 = I4 = I3 = I1= I0 =1 | 0 | 0 | 0 |
| Case 3:  All 8 inputs are equal to 0. | 0 | 0 | 0 |

Case 1:

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a circuit board

Description automatically generated

Make comment on results

E0 is in a HIGH state when E1 is in a low state, and not all of the inputs are in a

HIGH state.

When only A2 is in a high state, D0, D4, D5, D6, and D7 are currently in a high

state because the priority encoder initiates checking from D7. If D7 is in a high

state, the encoder proceeds to check other inputs, stopping when an input is in a

low state. Only A2 and E0 are in a high state, with D7 holding the priority..

Case 2:

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a circuit board

Description automatically generated

Make comment on results

Base on the case 1’s comment on case 1, D7 still holding priority. E0 is the only output show high.

Case 3:

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a circuit board

Description automatically generated

Make comment on results

The comment still the same as the previous response, D7 still priority, E0 is the only output show high

3. 2-to-4 Decoder - IC74HC139

Construct the circuit as below:

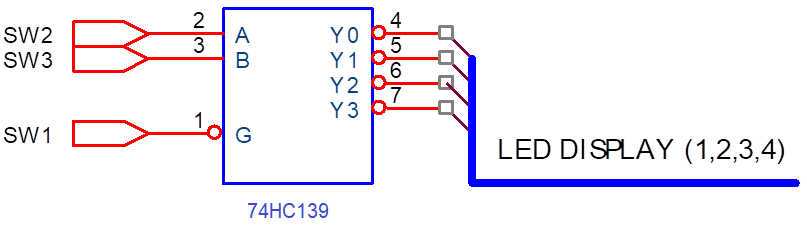


Figure 2 – Decoder 2-line-to-4-line IC 74HC139

- 4 outputs (Y0-Y3) are connected to LED display (Led 1-4).

- The data inputs (A, B) and control input (G) are connected to switches.

- Change the states of inputs to fulfill the truth table of IC 74HC139.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | Outputs | | | |
| Control | Data | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | X | X | 0 | 0 | 0 | 0 |

Implement the circuit via simulation software and paste the result in here

A computer diagram of a circuit board

Description automatically generated

Briefly describe the operation of the IC

The IC 74HC139 decodes two binary-weighted addresses from two inputs (A00, A01) into four distinct outputs (Y00 to Y03). Each decoder includes an enable input (E0), and when E0 is set to a HIGH state, all outputs are compelled to be in a HIGH state.

4. 3-TO-8 Decoder– IC 74HC138

Construct the circuit as below:

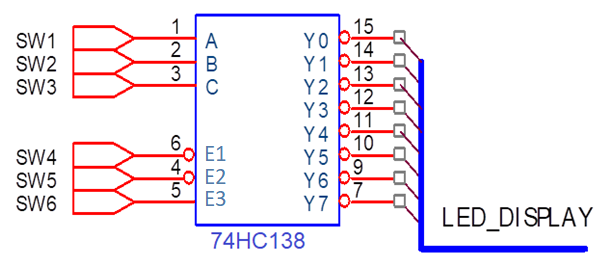


Figure 3 – 3-to-8 Decoder/demultiplexer - IC 74HC138

- 8 outputs are connected by using LEDs.

- The inputs are controlled by switches.

- Observe the results and fulfill the truth table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| INPUT | | | | | | OUTPUT | | | | | | | |
| E3 | E2 | E1 | C | B | A | Y0 | Y1 | Y2 | Y 3 | Y4 | Y 5 | Y 6 | Y7 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | 1 | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Implement the circuit via simulation software and paste the result in here

A computer diagram of a circuit board

Description automatically generated

Briefly describe the operation of the IC

The 74HC138 processes a three-bit binary-weighted address from inputs A0, A1, and A2. When enabled, it generates an active-low output, and the remaining seven outputs are set to a HIGH state

5. Design combinational circuits using decoders and OR gate

- Implement Boolean expression using IC 74HC138 & OR gate.

- The data inputs A, B, C are connected to switches.

- The control inputs are in suitable levels.

- Implement the circuit and verify the truth table

a.

Establish the truth table

|  |  |  |  |
| --- | --- | --- | --- |
| x | y | z | F |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Implement the circuit via simulation software and paste the result in here

A computer diagram of a circuit board

Description automatically generated

A computer screen shot of a circuit board

Description automatically generated

A computer diagram of a circuit board

Description automatically generated

Verify the truth table and make comment on the results

A diagram of a circuit

Description automatically generated

A diagram of a circuit

Description automatically generated

A diagram of a circuit

Description automatically generated

b.

F=x’yz + x(y+y’)(z+z’) +(x+x’)y’z’

…

F= x’yz+xyz+xy’z+xyz’+x’y’z’+xy’z’+ x’y’z’

Σf= (0,3,4,5,6,7)

Establish the truth table

|  |  |  |  |
| --- | --- | --- | --- |
| x | y | z | f |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

Implement the circuit via simulation software and paste the result in here

A computer diagram of a circuit board

Description automatically generated

A computer screen shot of a circuit board

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Description automatically generated

Verify the truth table and make comment on the results

- There are 6 high states of the output of IC 74HC138 & OR gate:

- In the first state x is low , y is low , z is low

- In the second state x is low, y is high, z is high

- In the third state x is high , y is low , z is low

- In the fourth state x is high , y is low, z is high

- In the firth state x is high , y is high, z is low

- In the sixth state x is high , y is high , z is high